raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. OBJECTIONS TO THE SPECIFICATION AND THE DRAWINGS

The Office Action objects to the specification and the drawings and asserts that there is no support for, and the drawings do not show, "a plurality of transistors disposed correspondingly to intersections between the data line and the scanning line" and "the channel region having a semiconductor portion protruding out of the channel region." Claim 1 has been amended for clarification.

Claim 1 has been amended to recite "a transistor disposed correspondingly to an intersection between the data line and the scanning line." Figs. 1-3 show a transistor TFT disposed correspondingly to an intersection between a data line 6a and a scanning line 3a. Support for this amendment is provided throughout the specification and at least at, e.g., page 8, lines 21-29 and page 9, lines 10-16.

Claim 1 has been amended to recite "a semiconductor portion protruding out of the channel region." ***Exemplary Fig. 3***, attached to this Amendment, illustrates a semiconductor portion (lower right side of 1a, or area adjacent contact hole 7) protruding out of the channel region (lower left side of 1a, or area above contact hole 5). Support for this amendment is provided throughout the specification and at least at, e.g., page 10, lines 12-20, and in Fig. 3.

Support for the subject matter in claim 1 is provided throughout the specification and Figs. 1-3, and at least at page 9, lines 10-22, page 10, lines 8-20. Withdrawal of the objections to the specification and the drawings are specifically requested.

II. CLAIMS 1-8 AND 20-21 SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, FIRST PARAGRAPH

The Office Action rejects claims 1-8 and 20-23[1] under 35 U.S.C. §112, first paragraph. The Office Action asserts that it is not clear where support for "a plurality of transistors disposed correspondingly to intersections between the data line and the scanning line" and "the channel region having a semiconductor portion protruding out of the channel region" is found in the specification. As mentioned above, claim 1 has been amended for clarification. Based on the discussion under Section I of this Amendment and the showing of support for these recited features in the specification and Figs. 1-3, withdrawal of this rejection is respectfully requested. See also Section III of this Amendment for a further explanation.

III. CLAIMS 1-7 AND 20-21 SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, SECOND PARAGRAPH

The Office Action rejects claims 1-8 and 20-21 under 35 U.S.C. §112, second paragraph.

The Office Action asserts that the recitation of "a plurality of transistors disposed correspondingly to intersections between the data line and the scanning line" is unclear. Claim 1 has been amended in accordance with the Examiners suggestion, i.e., to recite "a [single] transistor disposed correspondingly to an intersection between the data line and the scanning line."

The Office Action asserts that the recitation of "the channel region having a semiconductor portion protruding out of the channel region" is unclear. Claim 1 has been amended to recite " a semiconductor portion protruding out of the channel region and not being covered with the gate electrode" such that it is understood that the semiconductor portion (lower right side of 1a, or area adjacent contact hole 7) that protrudes out of the

[1] This rejection is moot as to claims 22-23 which were canceled in the January 31, 2003 Amendment.

channel region is different from the semiconductor portion (lower left side of 1a, or area above contact hole 5) that defines that channel region. See also Exemplary Fig. 3 attached to this Amendment.

The Office Action asserts that the recitation of "a contact hole" on line 10 of claim 1 is unclear because it refers to the same contact hole recited on line 9. In accordance with the Examiners suggestion, the "contact hole" at line 10 has been revised to recite --a second contact hole--.

Claim 1, and thus claims 2-8 and 20-21 which depend from claim 1, have been amended in conformity with 35 U.S.C. §112, second paragraph. Withdrawal of this rejection is respectfully requested.

IV. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects: claims 1, 3-7 and 20 under 35 U.S.C. §102(b) over U.S. Patent 5,614,730 to Nakazawa et al.; claim 2 under 35 U.S.C. §103(a) over Nakazawa et al. in view of U.S. Patent 5,316,960 to Watanabe et al.; claim 8 under 35 U.S.C. §103(a) over Nakazawa et al; and claim 21 under 35 U.S.C. §103(a) over Nakazawa et al. in view of JP 06163891 to Nishihara et al. Applicant respectfully traverses these rejections.

In particular, Applicant asserts that neither Nakazawa or Nishihara, alone or in combination, teach, suggest, or render obvious, an electro-optical device including a transistor disposed correspondingly to an intersection between the data line and the scanning line, the transistor including a gate electrode and a semiconductor layer, wherein the semiconductor layer comprises a source region that is connected to the pixel electrode through a contact hole, a drain region that is connected to the data line through a second contact hole, a channel region disposed under the gate electrode, and a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in claim 1.

The Office Action (at page 4, lines 6-10) provides that Nakazawa discloses in Figs. 19A-19C and 20 a semiconductor layer 102 having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate-length direction that is a direction in which one of the plurality of data lines extends. The construction of Nakazawa is substantially different from the construction of the Applicant's claimed invention. See, e.g., Fig. 19A of Nakazawa.

Claim 1 discloses the semiconductor layer including at least three parts. See, e.g., Figs. 2, 3 and 9 of the application. That is, a first part having a source region on the bottom side of the semiconductor having a contact hole 5. A second part is disclosed as having a drain region, shown at the upper and right side of the semiconductor layer having a contact hole 8, and a third part is disposed under the gate electrode. The third part has a portion protruding out of the gate electrode (channel region in the semiconductor layer).

Nakazawa discloses a first part (source) and a second part (drain). However, Nakazawa fails to teach or suggest a third part having a semiconductor portion that protrudes out of the gate electrode. As shown in Fig. 19A of Nakazawa, the right part (drain) of the semiconductor layer 102 has a contact hole 1905 corresponding to the second part, and the left part (source) of the semiconductor layer 102 has a contact hole 1906 corresponding to the first part. However, Nakazawa fails to teach or suggest that the third part (with contact hole 1904) having a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in independent claim 1. To the contrary, the semiconductor layer 102 is only shown disposed between the first part (source) and the second part (drain), and not "protruding out of the channel region and not being covered with the gate electrode," as recited in claims 1 and 24.

Furthermore, Nakazawa also discloses that the semiconductor layer 102 is located only at the region located adjacent to the gate electrode 103. However, Nakazawa fails to teach or suggest a semiconductor portion protruding out of the channel region and not being

covered with the gate electrode, as recited in independent claims 1 and 24. To the contrary, Nakazawa only teaches what is known conventionally (see the specification at col. 10, lines 14-16), i.e., that the semiconductor layer 102 does not extend toward the outside of the channel region of the semiconductor layer 1a. See, e.g., Fig. 19A of Nakazawa. In Fig. 19a of Nakazawa, only the end of the gate electrode 103 extends outside of the channel region, and not the semiconductor region 102 that forms the transistor.

Nishihara fails to make up for the deficiencies of Nakazawa disclosed above. In particular, Nishihara discloses in Figs. 7 and 8 portions of a scanning line 5 that form a gate electrode. In stark contrast to Applicant's claimed invention, Nishihara discloses that the lower end in the gate-length direction of the gate electrode 103 fails to teach or suggest a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in claims 1 and 24.

Wantanabe also fails to make up for the deficiencies of Nakazawa and Nishihara, discussed above either alone or in combination.

For at least these reasons, the applied references fail to teach, suggest, or render each and every feature as the claimed invention. Thus, Applicant asserts that independent claim 1 defines patentable subject matter. Claims 2-8 and 20-21 depend from the independent claim 1, and therefore also define patentable subject matter. Accordingly, Applicant respectfully request that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) be withdrawn.

V. NEW CLAIM

Claim 24 has been added and is also patentable for the reasons stated above. Claim 24 is similar to claim 1 but recites an electro-optical device including a "plurality" of elements.

VI. CONCLUSION

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

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JAO:HNS/cfr

Attachments:
Appendix
Exemplary Fig. 3

Date: June 11, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

Claim 24 is added.

The following is a marked-up version of amended claim 1:

1. (Thrice Amended) An electro-optical device, comprising:

a substrate;

a pixel electrode;

a scanning line;

a data line crossing the scanning line; and

a ~~plurality of~~ transistors disposed correspondingly to an intersections between the data line and the scanning line, ~~each of~~ the ~~plurality of~~ transistors including a gate electrode and a semiconductor layer, wherein the semiconductor layer comprises a source region that is connected to the pixel electrode through a contact hole, a drain region that is connected to the data line through a second contact hole, a channel region disposed under the gate electrode, and ~~the channel region having~~ a semiconductor portion protruding out of the channel region and not being covered with the gate electrode.